A model of technological progress in the microprocessor industry

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Abstract

This paper develops a model of technological progress in the microprocessor industry that connects the seemingly disparate engineering and economic measures of technological progress. Technological progress in the microprocessor industry is driven by the repeated adoption of higher quality vintages of capital equipment produced by the upstream semiconductor equipment industry. The model characterizes the optimal adoption decision of a microprocessor firm and the resulting rate of technological progress. In conjunction with parameters estimated using a new dataset of the microprocessor industry, the model suggests explanations for the acceleration in technological progress during 1990-2000 and the subsequent slowdown. (JEL: O31, L63)

1 Introduction

A number of studies seeking to explain the increase in productivity growth in the US economy during the second half of 1990s credit a central role to an acceleration in technological progress in the microprocessor industry.[1] The cause of the acceleration has been debated in many academic, industrial and policy forums.[2] The rate of technological progress in the microprocessor industry slowed down after 2000. There has been no convincing explanation of the acceleration or slowdown to date. Jorgenson (2001) points to the need for an economic model of technological progress in this industry to understand the cause of the acceleration. The multifaceted nature of technological progress in microprocessors has generated a plethora of characterizations of technological progress in this industry. Engineers favor a description based on Moore's law - a statement made in Moore (1975) that the number of transistors on a semiconductor chip doubles every two

[1] Jorgenson (2001) was the first to point out the importance of microprocessor industry. See also Oliner and Sichel (2002a) and Gordon (2002).

[2] See for example the proceedings of the workshop on Measuring and Sustaining the New Economy (2002), organized by the Board on Science, Technology and Economic Policy.

years.[3] Scientists prefer the rate at which the physical dimensions of an individual transistor has gone down, which has decreased by a factor of roughly 0.7 every 2-3 years. Business analysts in the semiconductor industry resort to the rate at which the processing speed (also called performance) of microprocessors have increased, while economists use the rate at which price per quality unit of microprocessors have declined.[4] By incorporating choices over engineering variables like transistor size and number of transistors, alongside economic variables like price, quantity and time of new technology adoption, the model in this paper successfully connects these disparate engineering and economic measures of technological progress.

The model also formalizes the commonly held notion in the industry that the key decision facing a microprocessor firm is when to adopt a new vintage of capital equipment. Once the adoption decision has been made, profit maximizing considerations dictate a clear choice of the size of transistor to use, the number of transistors to use, the processing speed and the price per quality unit. A contribution of this paper is the characterization of the adoption decision and the resulting time paths for the four variables. The optimal time to adopt new capital equipment is when the lag behind the best available capital equipment reaches a threshold value. This result has been previously obtained in other models of technology adoption, including Balcer and Lippman (1984), Dixit and Pindyck (1994), Doraszelski (2001), and Farzin, Huisman and Kort (1998).[5] The predictions of the model regarding the adoption policy and the time paths of the four measures of technological progress fit well with the empirical observations, which are outlined in section 2. The impor-

[3]A transistor is the basic electronic component in a microprocessor. See section 2 for more details. Moore (1965) predicted the number of transistors on a chip to double every year, which was later revised to doubling every two years in Moore (1975).

[4]Table 3 gives average growth rates for performance and price per quality unit.

[5]Although not directly related, this paper is in the spirit of Griliches (1957), who uses a model of technology adoption to understand the causes of variation in hybrid corn adoption pattern across different states in the US during 1932-1956. In a similar vein, this paper uses a model of technology adoption to understand the cause of the acceleration and slowdown that occurred in the rate of technological progress in the microprocessor industry during 1971-2008. For a good survey of models of technology adoption, see Hoppe (2002).

tance of the adoption of new capital equipment highlights the fact that technological progress in microprocessors is driven to a large extent by innovations in the upstream semiconductor equipment industry.[6] Semiconductor equipment firms like Nikon, Canon, Applied Materials and ASML invent new generations of capital equipment which allow microprocessor firms like INTEL and AMD to fabricate smaller transistors, enabling them to make higher performance microprocessors. The notion that the repeated adoption of higher quality vintages of capital equipment is the driver of technological progress in the microprocessor industry has been emphasized in Aizcorbe and Kortum (2005).

A distinguishing feature of this paper is that it models technology in the industry in more detail than is common in economic models. This more detailed incorporation of the technology turns out to be essential to understand the causes of the acceleration and slowdown in technological progress, because it helps to separate out the contribution of the semiconductor equipment firms from that of microprocessor firms towards technological progress in the microprocessor industry. There have been many previous studies of the acceleration and slowdown, including Jorgenson (2001), Aizcorbe (2005), Aizcorbe, Oliner and Sichel (2006) and Flamm (2004). The studies above characterize the rate of technological progress in terms of the rate at which price per quality unit has declined for microprocessors.[7] This approach however has the limitation, as noted in Aizcorbe et al. (2006), that changes in prices brought about by changes in demand and competitive conditions can be mistakenly attributed to changes in the rate of technological progress. To overcome this problem, I use the notion of technological progress as the growth of microprocessor performance.[8] Performance, or processing speed, is a measure of how fast a microprocessor can execute software programs. Nordhaus (2001) gives a detailed description of the use of performance as a measure of technological progress in computing, and compares it with the hedonic price based approach.

[6] Section 2 elaborates on this link between technological progress in the microprocessor industry and the adoption of new vintages of capital equipment.

[7] The price per quality unit is estimated using hedonic regressions.

[8] Performance is the commonly used measure for comparing microprocessors in computer science. It is the reciprocal of the time that the microprocessor takes to execute a given set of software programs.

Figure 1 shows the performance of microprocessors produced by two main microprocessor companies, INTEL and AMD, during 1971-2008. As the figure shows, growth rate of performance increased during 1990-2000 and decreased subsequently. Table 3 shows the magnitude of the increase in growth rate of performance and compares it with the growth rate of price per quality unit declines mentioned in Aizcorbe et al. (2006). As can be seen from Table 3, the growth of performance closely follows the hedonic price based measure of technological progress.

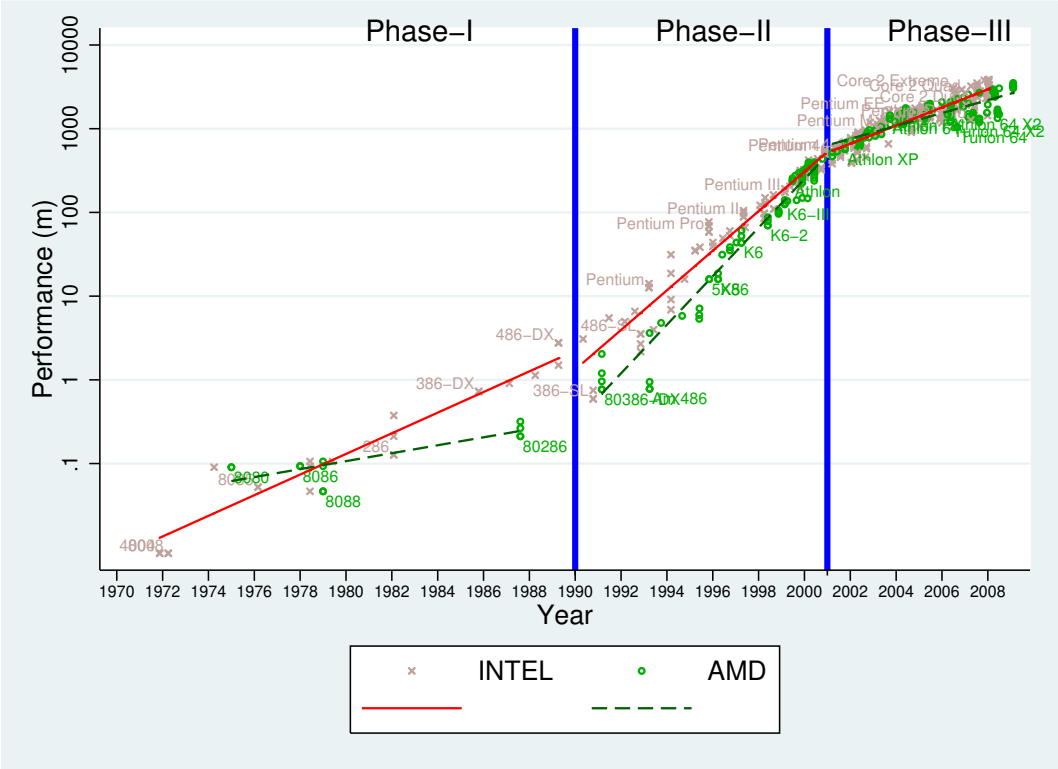


Figure 1: The Acceleration and Slowdown for INTEL and AMD.

The model in this paper implies that in steady state, the mean growth rate of performance is determined by two parameters, the rate of innovation in the upstream semiconductor equipment industry and the efficiency with which a microprocessor firm uses these upstream innovations (see

section 3.3 for a description of efficiency in this industry). The model, together with empirical estimates of the parameters, imply that the acceleration during 1990-2000 was caused by an increase in the innovation rate in the upstream semiconductor equipment industry, while the slowdown after 2000 was caused by a decrease in the efficiency with which the microprocessor industry used the upstream innovations. In a nutshell, the upstream semiconductor equipment firms were responsible for the acceleration and the downstream microprocessor firms for the slowdown. These explanations also find support in previous papers. Jorgenson (2001) suggests that the acceleration was caused by a decrease in the technology cycle in the semiconductor equipment industry from 3 yrs to 2 yrs, a fact confirmed in Figure 2. An increase in the innovation rate in the semiconductor equipment industry leads to a decrease in the technology cycle, as shown in section 5 in this paper. Aizcorbe et al. (2006) also find support for the explanation in Jorgenson (2001), but they remain cautious about this explanation because the innovation rate did not drop during the period of the slowdown. This paper provides the missing link in the explanation. Even though the innovation rate in the semiconductor equipment industry did not drop, there was a drop in the efficiency with which microprocessor firms used these innovations during the slowdown period.

The slowdown since 2000 has reduced the contribution of the microprocessor industry to aggregate productivity growth. The impact of the acceleration and slowdown on total factor productivity (TFP) growth in the US economy can be calculated using the method suggested in Oliner and Sichel (2002a). In their method, the aggregate TFP growth is the weighted average of the TFP growth in the different sectors in the economy, where the weight for each sector is its gross output as a share of the aggregate output.[9] Using the growth rate of performance as a proxy for the TFP growth rate in the microprocessor industry, Table 5 shows that the contribution of microprocessor industry to aggregate TFP growth quadrupled during the acceleration and more than halved during the slowdown. This paper suggests that technological progress in the microprocessor in-

[9]The theoretical justification for the method is given in Hulten (1978). Note that this method captures only the direct contribution of production of microprocessors to aggregate TFP growth, and omits the indirect effect through the use of better computers made possible by faster microprocessors.

dustry is unlikely to return to the accelerated path during 1990-2000, unless the industry finds a way to increase the efficiency with which it is using the innovations generated by the semiconductor equipment industry. I now turn to a brief description of the connection between technological progress in the microprocessor industry and innovations in the upstream semiconductor equipment industry.

2 Technological Progress in the Microprocessor Industry - the link to the Semiconductor Equipment Industry

A microprocessor can be thought of as a collection of transistors which operate in tandem to execute instructions contained in different software programs. The performance of a microprocessor can be increased either by increasing the speed of operation of each individual transistor or by using more transistors so that more software instructions can be executed simultaneously (in parallel). The speed of operation of each individual transistor is limited by its size, smaller transistors are faster. The size of each transistor is in turn limited by the quality of the capital equipment used in manufacturing the microprocessor. Innovations in the semiconductor equipment industry lead to capital equipment that can make smaller transistors.[10] The evolution of the microprocessor industry towards faster microprocessors traces the repeated adoption of higher quality vintages of capital equipment produced by the semiconductor equipment firms, each vintage of capital equipment being marked by the size (or length) of the transistor that the equipment allows the microprocessor industry to make. Since these transistor sizes are really small, they are usually quoted in microns (μ), which is a millionth of a meter. The leading microprocessor firm, INTEL, has adopted four-

[10]The equipment industry has a separate classification under the North American Industrial Classification System (NAICS Code 333295). Some of the important firms in this industry are Applied Materials, Tokyo Electron, Nikon, Canon, ASML, Terdayne and Advantest. VLSI Research, a market research organization focussing on the semiconductor industry estimates the total revenue for the equipment industry in 2007 to be 57.5 billion dollars, 67% of which was accounted for by the top 15 companies. (See Semiconductor-International (2008).)

teen such vintages during 1971-2008, 10μ, 6μ, 3μ, 1.5μ, 1μ, 0.8μ, 0.6μ, 0.35μ, 0.25μ, 0.18μ, 0.13μ, 0.09μ, 0.065μ and 0.045μ. Figure 2 plots the different vintages of semiconductor capital equipment that INTEL and AMD have adopted against the date of adoption. In the progression

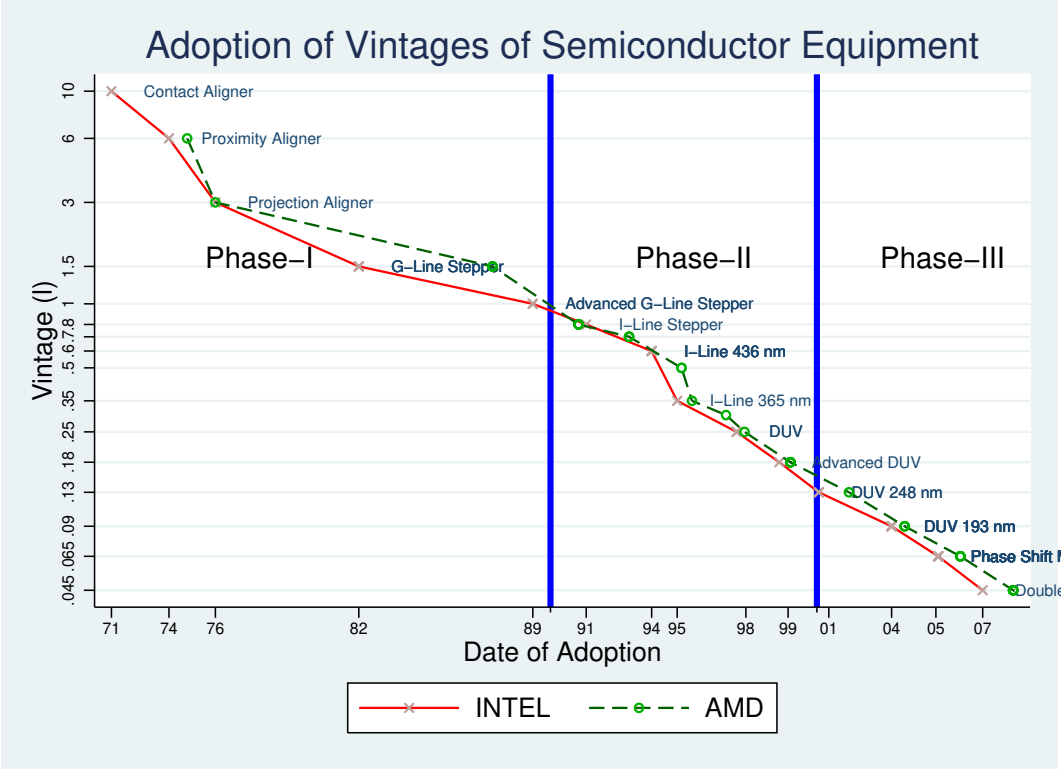


Figure 2: INTEL and AMD's adoption of new vintages of semiconductor capital equipment.

Notes: The date of adoption of a vintage is taken to be the date on which INTEL (or AMD) released the first microprocessor manufactured with that vintage. The dates marked on the x-axis are Intel's adoption dates. Note the decrease in the average time interval between adoptions after Phase I. This is the reduction in technology cycle that has been noted in Jorgenson (2001), Aizcorbe et al. (2006) and Flamm (2004).

through these fourteen vintages from 1971 to 2008, the transistor size has decreased by a factor of 222. I use the letter ℓ to denote the vintage of capital equipment which can produce transistors

of size ℓ. A lower ℓ thus implies a higher quality vintage. Equipped with this brief introduction to technology in the microprocessor industry, I document below four stylized facts about the evolution of the four measures of technological progress in the microprocessor industry mentioned in the introduction. I denote the time period 1971-1989 as Phase I, the period 1990-2000 as Phase II and the period 2001-2008 as Phase III.[11] The four stylized facts are:

1. The adoption of each new vintage of capital equipment decreases the transistor size ℓ by roughly the same factor (see Figure 4). For brevity, I will call this as the *scaling factor*.

2. The number of transistors in a microprocessor, T, increases at roughly double the rate at which transistor size ℓ decreases (see Figure 5).

3. Performance grows at a roughly constant rate within each phase. The average growth rate of performance almost doubled going from Phase I to Phase II (the acceleration) and more than halved going from Phase II to Phase III (the slowdown). (See Figure 1 and Table 3.)

4. Price/Performance (price per quality unit) declines at a roughly constant rate within each phase. The average decline rate of price/performance increased going from Phase I to Phase II (the acceleration) and decreased going from Phase II to Phase III (the slowdown). (See Table 3.)

The next section develops a model that is consistent with the pattern of evolution of the four measures of technological progress documented in the stylized facts above.

3 The Model

The model is in continuous time. I develop the model in a few stages starting with the semiconductor equipment industry.

[11] This section, and the other empirical sections of this paper, uses a new dataset of the microprocessor industry that has been created using data from a variety of sources. See data appendix for a description of the data sources.

3.1 The Semiconductor Equipment Industry

Although the semiconductor equipment industry consists of a large number of firms which manufacture different types machinery, from the point of view of technological progress in the microprocessor industry the most important function that these companies serve is that they undertake the R&D necessary to manufacture the next vintage of capital equipment. Hence I lump all these companies together as the semiconductor equipment industry. I denote the frontier or highest quality vintage (i.e. the vintage with the smallest transistor size) by $\bar{\ell}$. The R&D done by the semiconductor equipment industry generates innovations that follow a Poisson process with parameter λ. Each innovation reduces $\bar{\ell}$ by a fixed factor δ, where $\delta < 1$. Hence the stochastic process for $\bar{\ell}$ can be written as

$$\bar{\ell}(t) = \delta^{N(t)}\bar{\ell}(0),$$

$$N(t) \; is \; a \; Poisson \; process \; with \; rate \; \lambda.$$

I now turn to a description of the demand side of the model.

3.2 Demand in the Microprocessor Industry

Consumers care only about the performance of microprocessors. I assume a stationary inverse demand curve, given by,

$$\frac{p(t)}{m(t)} = D\left\{m(t)y(t)\right\}^{\frac{-1}{\eta}}. \tag{1}$$

Here $p(t)$ is the price of microprocessor sold at time t, $m(t)$ is the performance (quality) of the microprocessor and $y(t)$ is the number of microprocessors demanded. The price per quality unit is $\frac{p(t)}{m(t)}$, and $m(t)y(t)$ is the total number of quality units demanded. The basic assumption behind the demand structure is that total quality units demanded has a constant elasticity, η, in price per quality unit. One obvious abstraction in this demand specification is the absence of dynamic decision making by forward looking consumers. It is unlikely that a change in dynamic decision

making process by consumers could have been a cause of the acceleration and slowdown, so I ignore this aspect of demand.[12] I now describe the technology side of the model.

3.3 Technology in the Microprocessor Industry

A microprocessor firm like INTEL chooses the quality (performance) of its product to maximize profits. The common way to model the quality choice of a firm is to have the firm pay a fixed cost to obtain an improvement in quality (e.g. in Sutton (2001).[13]. The production process in the microprocessor industry, however, gives rise to a peculiar tradeoff between performance and costs not captured in such models. Equations (2) and (3) below, which capture the central aspects of production technology in the microprocessor industry, illustrate this tradeoff. A firm in the microprocessor industry has two ways to increase the performance of its microprocessor. First, it can adopt a new vintage of capital equipment which enables it to fabricate smaller (lower ℓ) and hence faster transistors.[14] Second, it can increase the number of transistors that it uses in its microprocessor, which allows the firm to fabricate more units working in parallel in the microprocessor, thus increasing performance. Performance can thus be written as a function of the number of transistors T and the vintage of capital equipment ℓ,

$$m(T, \ell) = \frac{T^{\alpha}}{\ell}. \tag{2}$$

[12] See Gordon (2009) for a model of dynamic decision making and replacement cycles in the microprocessor industry.

[13] In other models, like Pakes and McGuire (1994), paying the fixed cost increases the probability of making an improvement in quality.

[14] Reducing ℓ by a given factor increases the speed of each transistor by the same factor (see Ronen, Mendelson, Lai, Lu, Pollack and Shen (2000) or Borkar (1999)) and hence increases the performance m of the microprocessor by the same factor. "Every new process generation brings significant improvements in all relevant vectors. Ideally, process technology scales by a factor of 0.7 all physical dimensions of devices (transistors) and wires (interconnects) .... . With such scaling, typical improvement figures are the following: 1.4-1.5 times faster transistors; two times smaller transistors...", Ronen et al. (2000). The names "process generation" and "process technology" in the above quote are terms used in the semiconductor industry to refer to vintages of capital equipment.

A microprocessor firm has the choice of increasing performance by increasing the number of transistors, without having to reduce ℓ by adopting a new vintage of capital equipment. Such an approach, however, increases the marginal cost of producing a microprocessor because it increases the fraction of microprocessors that are defective in any lot, a feature stemming from the peculiarities of the semiconductor production process. In any given lot of microprocessors manufactured, a certain fraction would be defective because of manufacturing imperfections arising from contamination by dust particles in the course of production. The fraction of defective microprocessors increases with the physical area A of the microprocessor because larger microprocessors have a higher probability of being contaminated by dust particles. A commonly used *yield* model in the industry gives the fraction of good microprocessors in any given lot as e^{-A}, where A is the area of the microprocessor.[15] Hence, if $\bar{c}$ is the unit cost of producing a raw microprocessor, the marginal cost of producing a good microprocessor is $\bar{c}e^{A}$. Since the area of each individual transistor is ℓ^2, the area the microprocessor containing T transistors is $A = T\ell^2$. Substituting for A, the marginal cost is given by,

$$c(T, \ell) = \bar{c}e^{T\ell^2} \tag{3}$$

Increasing T without reducing ℓ rapidly escalates the marginal cost. If the firm reduces ℓ by adopting a new vintage and increases T in proportion to $\frac{1}{\ell^2}$, then the marginal cost remains constant while performance increases. This is indeed the policy that the model in this paper predicts to be the optimal policy, as well the policy that microprocessor firms have followed in practice (see stylized fact 2 and Figure 5). Although adopting a new vintage allows a microprocessor firm to keep marginal cost constant while increasing performance, the firm has to expend a considerable amount

[15]The formula for the fraction good microprocessors (*yield*) used in this paper, e^{-A}, is called the Poisson yield equation. The Poisson yield is usually given as $e^{-\sigma S}$, where σ is a parameter that captures the degree of manufacturing imperfections, and S is the physical area of the microprocessor. For the purposes of this paper, $A = \sigma S$, can be thought of as the effective area, which takes into account the multiplication by σ. See Berglund (1996) for a description of yield models in the semiconductor industry.

of engineering effort in perfecting the production process with the new vintage of machines.[16] I capture this fixed cost with the function $F(\ell)$, which increases as ℓ decreases. The fixed cost $F(\ell)$ does not include the user cost of capital, which is incorporated into the unit cost of producing a raw microprocessor, $\bar{c}$.

The functions $m(T, \ell)$, $c(T, \ell)$ and $F(\ell)$ capture the technology in this industry. Note that in the function $m(T, \ell)$ in equation (2), the ability of a microprocessor firm to translate increases in T to increases in m depends on the parameter α. The parameter α is a measure of quality of design used in the microprocessor. With a superior design (higher α), a microprocessor firm can get bigger performance increments from a given increase in the number of transistors. This design quality is thus a measure of the technical *efficiency* of the microprocessor firm. In section 5, I argue that a drop in efficiency α caused the slowdown in technological progress in the industry. Using the primitives of demand and technology in sections (3.2) and (3.3), the next section lays down the profit maximization problem faced by a microprocessor firm.

3.4 The Profit Maximization Problem of the Microprocessor Firm

Before turning to formal description of the microprocessor firm's problem, I make two assumptions. First, I assume that the market for microprocessors consists of a single firm facing the demand curve in equation (1). Although there are two major microprocessor producers, INTEL and AMD, INTEL has been at the forefront of making innovations in the industry while AMD has usually lagged behind. INTEL has also occupied 75%-90% of the microprocessor market during the time period considered in this paper. Moreover, in a paper exploring whether AMD spurs INTEL to innovate, Goettler and Gordon (2009) find that innovation is more in an INTEL monopoly than in an INTEL-AMD duopoly. In the light of these arguments, modeling the industry as a duopoly would complicate the analysis while providing little help in finding explanations of the acceleration and slowdown. Second, I assume that the microprocessor firm sells only the highest

[16] INTEL has estimated the cost of adoption next vintage of capital equipment (0.032μ) to be 7 billions dollars. See Condon (2009)

quality (performance) microprocessor. As soon as a better product is made, the entire production is moved to the new product. This assumption helps focus on the factors that determine the rate at which microprocessor performance is growing.

Given the Poisson arrival rate λ of innovations to capital equipment, each of which reduce $\bar{\ell}$ by a factor δ, the microprocessor firm has to choose the time paths of performance, marginal cost, the number of microprocessors to produce, the vintage of capital equipment to use, and the sequence of times at which to adopt new vintages of capital equipment, $\{\tau_j\}_{j=0}^{\infty}$. The choice of performance and marginal cost can equivalently be stated in terms of choice of number of transistors and vintage of capital equipment. Formally, the problem of the microprocessor firm is,[17]

$$\max_{T(t),\ell(t),y(t),\{\tau_j\}_{j=0}^{\infty}} \quad E\left[\int_0^{\infty} e^{-\rho t}\left[p(t)-c(T,\ell)\right]y(t)\,dt \;-\sum_{j=0}^{\infty} e^{-\rho\tau_j}F(\ell(\tau_j))\right]$$

$$subject\ to \qquad \frac{p(t)}{m(T,\ell)} = D\{m(T,\ell)y(t)\}^{\frac{-1}{\eta}},$$

$$m(T,\ell) = \frac{T^{\alpha}}{\ell}, \quad c(T,\ell) = \bar{c}e^{T\ell^2}$$

$$\ell(t) \geq \bar{\ell}(t), \quad \bar{\ell}(0) \ \ given,$$

$$\bar{\ell}(t) = \delta^{N(t)}\bar{\ell}(0), N(t)\ is\ a\ Poisson\ process\ with\ rate\ \lambda.$$

The term in the outer square brackets is the present discounted value of net profits, which is the difference between the present discounted values of gross profits (the integral term in the objective function) and the sum of fixed cost of adopting new vintages (the summation term in the objective function). The first constraint is the demand curve in equation (1), the second and third are the technology constraints in equations (2) and (3), the fourth simply states that the firm can at best

[17]To avoid notational clutter, I have abbreviated $m(T(t),\ell(t))$ as $m(T,\ell)$ and $c(T(t),\ell(t))$ as $C(T,\ell)$ in the statement of the problem.

be using the best vintage currently available, and the last specifies the stochastic process for the evolution of the best (frontier) vintage. I restrict $\eta > 1$ to make the firm's problem well defined.

3.5 Microprocessor Firm's Optimal Policies

The optimal choice of T and y depend only on the current value of ℓ. Hence I solve the problem by first solving the static problem of choosing T and y for a given ℓ and then embedding this solution back into the problem, to solve the dynamic problem of choosing the optimal times $\{\tau_j\}_{j=0}^{\infty}$ at which to adopt new ℓ. Substituting the constraints into the objective function, it can be seen that the solution to the static problem is as follows. Along an optimal path of T and y, the following condition has to hold,

$$T^*(\ell) = \alpha \frac{1}{\ell^2}. \tag{4}$$

Substituting equation (4) into equation (3) gives marginal cost as

$$c^*(\ell) = \bar{c}e^{\alpha} \equiv c^*. \tag{5}$$

The firm's optimal policy is thus to choose T in proportion to $\frac{1}{\ell^2}$ and hence keep the marginal cost at $c^* = \bar{c}e^{\alpha}$, irrespective of the vintage ℓ used. The optimality conditions in equations (4) and (5) result from the tradeoff between performance and marginal cost explained in section 3.3. Substituting equation (4) into equation (2) gives the optimal performance as,

$$m^*(\ell) = \frac{T^*(\ell)^{\alpha}}{\ell} = \alpha^{\alpha} \frac{1}{\ell^{1+2\alpha}}. \tag{6}$$

i.e. performance grows at $1 + 2\alpha$ times the rate at which ℓ decreases. The term $1 + 2\alpha$ shows the twin benefits that a microprocessor firm gets from using a vintage with a smaller ℓ. The exponent 2α represents the indirect benefit of smaller ℓ on m through T, and the exponent 1 represents the direct benefit arising from the fact that smaller transistors are faster. The optimal number of microprocessors to produce $y^*(\ell)$ is,

$$y^*(\ell) = (\eta - 1) \frac{1}{\bar{c}e^{\alpha}} \frac{\pi}{\ell^{\varphi}}. \tag{7}$$

where π and φ are given by,

$$\pi = \left((\eta-1)\frac{\alpha^\alpha}{\bar{c}e^\alpha}\right)^{\eta-1}\left(\frac{D}{\eta}\right)^\eta, \tag{8}$$

$$\varphi = (1+2\alpha)(\eta-1). \tag{9}$$

Substituting the solutions for m and y into the demand equation (1) gives the optimal price as,

$$p^*(\ell) = \frac{\eta}{\eta-1}\left[\bar{c}e^\alpha\right] \equiv p^*, \tag{10}$$

i.e. the price of a microprocessor is a constant markup over the marginal cost of production, the term inside square brackets being the marginal cost of production. The solutions p^* and $y^*(\ell)$ give the revenue along the optimal path as

$$r^*(\ell) = \eta\frac{\pi}{\ell^\varphi}. \tag{11}$$

As expected for a constant elasticity demand curve, the gross profit is a constant fraction $\frac{1}{\eta}$ of revenue, and is given by

$$\pi^*(\ell) = \frac{\pi}{\ell^\varphi}. \tag{12}$$

Using the gross profit function in equation (12), the microprocessor firm's problem can be rewritten as

$$\max_{\ell(t),\{\tau_j\}_{j=0}^\infty} \quad E\left[\int_0^\infty e^{-\rho t}\pi^*(\ell(t))\,dt \; - \sum_{j=0}^\infty e^{-\rho\tau_j}F(\ell(\tau_j))\right]$$

$$\begin{aligned} \textit{subject to} \qquad & \pi^*(\ell(t)) = \frac{\pi}{\ell(t)^\varphi}, \\ & \ell(t) \geq \bar{\ell}(t),\ \bar{\ell}(t) = \delta^{N(t)}\bar{\ell}(0), \\ & N(t)\ \textit{is a Poisson process with rate}\ \lambda. \end{aligned}$$

I solve the problem using dynamic programming. The dynamic programming problem is most conveniently expressed by choosing the state variables as $\bar{\ell}$, the frontier vintage, and $x = \frac{\bar{\ell}}{\ell}$, which captures how far the firm is behind the frontier. Note that $x \leq 1$, since the firm can adopt a vintage no smaller than $\bar{\ell}$. Since the innovation arrival is Poisson, the probability of one innovation

arriving in a small interval of time Δt is $\lambda \Delta t$, and the probability of more than one innovation is approximately zero. Hence the value function should satisfy the Bellman equation,

$$V(\bar{\ell}, x) = \frac{\pi}{\left(\frac{\bar{\ell}}{x}\right)^{\varphi}} \Delta t \quad + \quad e^{-\rho \Delta t} \left[(1 - \lambda \Delta t) V(\bar{\ell}, x) \right.$$

$$\left. + \quad \lambda \Delta t \, Max \left\{ V(\delta \bar{l}, \delta x), V(\delta \bar{\ell}, 1) - F(\delta \bar{\ell}) \right\} \right].$$

The first term on the right hand side is the profit that the firm receives in a small interval of time Δt, the second term is the discounted expected payoff after Δt. With probability $1 - \lambda \Delta t$ no innovations arrive in which case the firm's value remains at $V(\bar{\ell}, x)$. With probability $\lambda \Delta t$ one innovation arrives, in which case the firm has to choose between not adopting this innovation and getting value $V(\delta \bar{\ell}, \delta x)$ or adopting it and getting a value $V(\delta \bar{\ell}, 1) - F(\delta \bar{\ell})$.

I assume that $F(\ell)$ is homogeneous of degree $-\varphi$, the same degree of homogeneity as the gross profit function, $\pi^*(\ell)$. If this were not true, then one would get a non-stationary model. If $F(\ell)$ was increasing at a faster rate in ℓ than $\pi^*(\ell)$, then the factor by which ℓ scales at each adoption (the scaling factor) would decrease over time, getting closer to 0. If If $\pi^*(\ell)$ was increasing at a faster rate than $F(\ell)$, then the scaling factor would increase over time, getting closer to 1. However, as Figure 4 shows, the scaling factor does not show any systematic variation over time, consistent with the assumption that $F(\ell)$ is homogeneous of degree $-\varphi$. The assumption that $F(\ell)$ is homogeneous of degree $-\varphi$ implies that $V(\bar{\ell}, x)$ is homogenous of degree $-\varphi$ in $\bar{\ell}$, and hence $V(\bar{l}, x) = \bar{l}^{-\varphi} V(1, x) = \bar{\ell}^{-\varphi} v(x)$, where $V(1, x) = v(x)$. The dynamic program can thus be expressed with a single state variable, x. Re-writing with the single state variable, and taking the limit $\Delta t \to 0$, the Bellman equation simplifies to,

$$\rho v(x) = x^{\varphi} \pi + \lambda \left[\frac{1}{\delta^{\varphi}} Max \left\{ v(\delta x), v(1) - F(1) \right\} - v(x) \right]. \tag{13}$$

The left hand side of the equation is the payoff to owning the firm, which is the sum of the instantaneous payoff and the change in value which occurs if an innovation arrives, an event with hazard λ (taking account of the option to adopt). The optimal policy is to adopt a new vintage when the

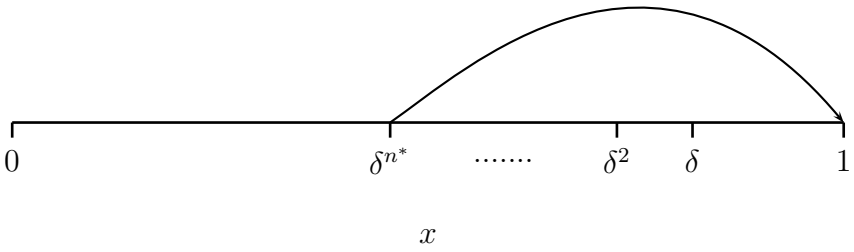
lag behind the frontier x, reaches a threshold values x^* (see Proposition 1 for proof). The threshold value x^* satisfies the following equation,

$$\rho(v(1) - F(1)) = \pi x^{*\varphi} + \lambda \left\{ \frac{1}{\delta^{\varphi}} \left[v(1) - F(1) \right] - \left[v(1) - F(1) \right] \right\}. \tag{14}$$

Equation (14) is the value matching condition mentioned in Dixit and Pindyck (1994) and Farzin et al. (1998). The firm adopts at the point where the value to adopting is equal to the value to waiting. The value to adopting immediately is the left hand side of the equation, the firms jumps to the frontier but it has to pay the fixed cost $F(1)$. The term on the right hand side is the value to waiting which is the sum of the instantaneous payoff and the change in value that occurs if an innovation arrives at that moment in time. Equation (14) can be rewritten to give the threshold value x^* as,

$$x^* = \left\{ \left(\rho + \lambda - \frac{\lambda}{\delta^{\varphi}} \right) \left(\frac{v(1) - F(1)}{\pi} \right) \right\}^{\frac{1}{\varphi}}. \tag{15}$$

Equation (15) requires $\rho > \lambda(\frac{1}{\delta^{\varphi}} - 1)$.[18] Since each innovation shrinks $\bar{\ell}$ by δ, this implies that it is optimal to adopt at every n^*th innovation, where n^* is the smallest integer such that $\delta^{n^*} \leq x^*$. It is easy to summarize the dynamic policy using the simple diagram below. The possible values of



x are $1, \delta, \delta^2, ..., \delta^{n^*-1}$. Starting from $x = 1$, the value of x decreases to δ, δ^2,.., as the equipment sector produces its stream of innovations. When the n^*th innovation arrives, the firm adopts it and x becomes equal to one again. This cycle repeats.

I summarize the results above. The microprocessor firm adopts every n^*th innovation made by the semiconductor equipment industry and hence ℓ used by the firm scales repeatedly by the same

[18] If discount factor ρ is not high enough, then discounted net profits are increasing over time and there will be no solution to the firm's problem.

factor δ^{n^*}. As ℓ decreases, the firm chooses to increase transistor count (T) and performance (m) in proportion to $\frac{1}{\ell^2}$ and $\frac{1}{\ell^{(1+2\alpha)}}$ respectively. The firm chooses to maintain the marginal cost at c^* and charge a price p^* per microprocessor, while increasing the number of units produced (y) in proportion to $\frac{1}{\ell^{\varphi}}$, where $\varphi = (1+2\alpha)(\eta-1)$. Revenue and gross profits also increase in proportion to $\frac{1}{\ell^{\varphi}}$. This concludes the development of model.

4 Discussion

In this section I show that the model's predictions are consistent with the stylized facts documented in section 2 and use the model to connect the four measures of technological progress mentioned in the introduction. The optimal choices of the firm with regard to engineering variables like number of transistors and performance as well as economic variables like quantity, profits and revenue are determined by the vintage ℓ of capital equipment that the firm is using, and evolves with the change in ℓ at each new vintage adoption. The model thus formalizes the commonly held notion in the microprocessor industry that the adoption of new vintages of capital equipment is the key driving force in the industry.

The model predicts that at the adoption of each new vintage, the transistor size ℓ should scale by the same factor δ^{n^*}, accounting for stylized fact 1. As equation (4) shows, the model predicts that the firm's optimal policy is to increase T in proportion to $\frac{1}{\ell^2}$, accounting for stylized fact 2. I show below that the mean growth rate of m is given by

$$g_m = -(1+2\alpha)\lambda \ln(\delta). \tag{16}$$

Thus the mean growth rate of m is constant as long as α and λ does not change. I argue in section 5 that changes in g_m between the three phases were caused by shifts in λ and α. Within each phase, with λ and α fixed, the model predicts that the mean growth rate of m is constant, accounting for stylized fact 3. Since price p does not change over time, the model predicts that price/performance ($\frac{p}{m}$) declines inversely with m, accounting for stylized fact 4. The model makes

one more testable prediction, that the microprocessor firm should adopt only occasionally, and should skip some innovations. In Figure 3, I plot the vintages adopted by INTEL (solid horizontal lines). The dotted lines are some of the vintages for which capital equipment was sold by some of the leading semiconductor equipment producers, but were not used by INTEL.[19] As can be seen from the graph, there were quite a number of vintages which INTEL did not adopt, in line with the prediction of the model.

The model connects the four measures of technological progress mentioned in the introduction. Since the firm's policy is to adopt every n^*th innovation, the mean growth rate of ℓ will be determined by the stochastic process generating the innovations. Since the innovations follow a Poisson process with rate λ and stepsize δ, the mean growth rate of ℓ is given by $g_\ell = \lambda \ln(\delta)$.[20] From equation (4) it is clear that T increases at twice the rate at which ℓ decreases, i.e. $g_T = -2\lambda \ln(\delta)$. From equation (6) it follows that $g_m = -(1 + 2\alpha)g_\ell$. This gives the mean growth rate of m as, $g_m = -(1 + 2\alpha)\lambda \ln(\delta)$. Finally, since the price of a microprocessor remains constant over time, the price per performance decreases at the rate at which performance increases, i.e. $g_{pm} = (1 + 2\alpha)\lambda \ln \delta$. The four expressions above bring out the relationships between the four measures of technological progress in the industry. While the rate of reduction in transistor size (g_ℓ) and growth in number of transistors per microprocessor (g_T) is fixed by the innovation parameters λ and δ in the upstream semiconductor equipment industry, the rate of growth of performance (g_m) and price/perperformance (g_{pm}) depend also on the the efficiency α with which the microprocessor firm uses the upstream innovations.

[19] The vintages for the dotted lines were produced by one of the following equipment companies - ASML, Nikon, GCA, SVGL, Parkin-Elmer and Ultratech.

[20] Note that $g_\ell < 0$ since $\delta < 1$.

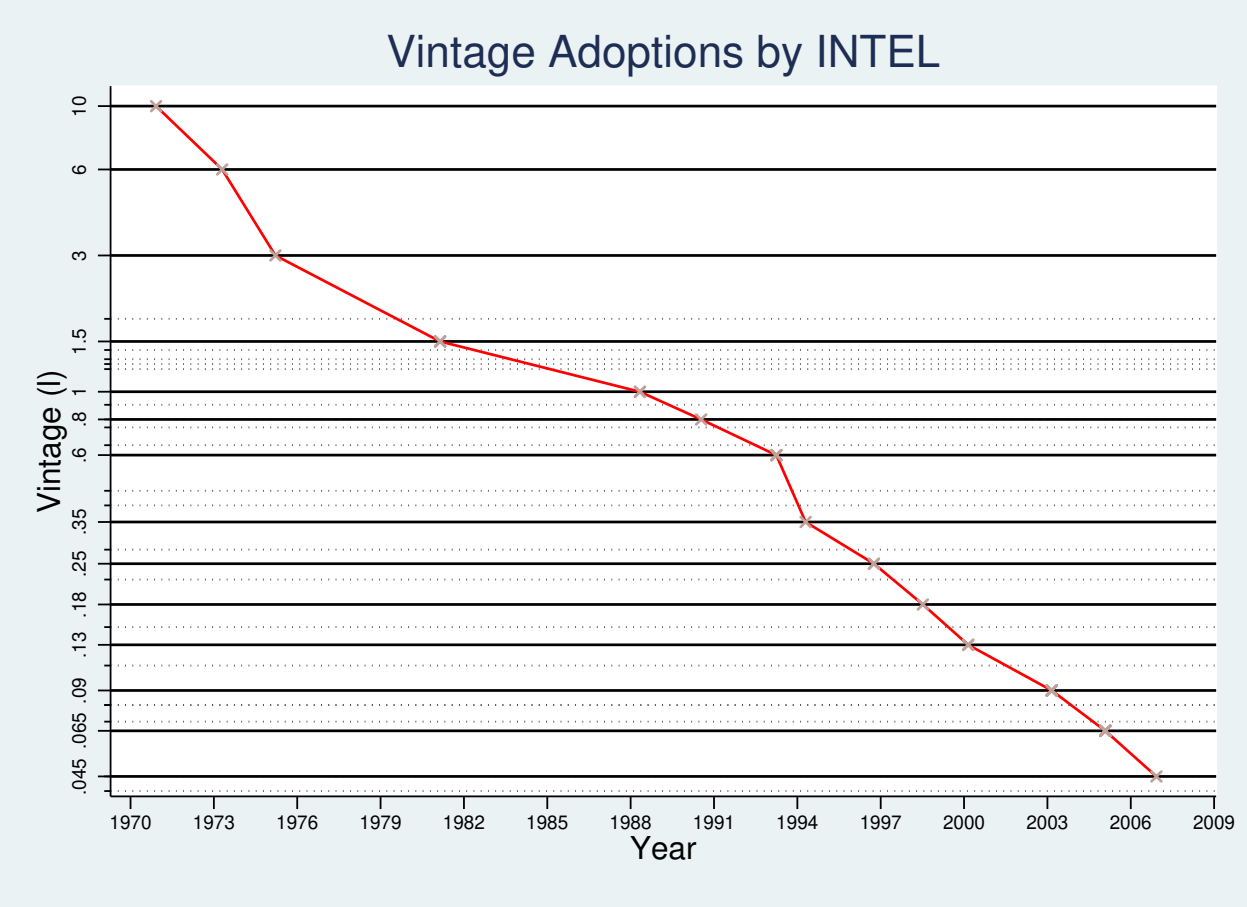


Figure 3: INTEL does not adopt all vintages.

Notes: The solid lines are vintages that were adopted by INTEL. The dotted lines are vintages that were produced by semiconductor equipment firms but were not adopted by INTEL. In line with the prediction of the model, INTEL does not adopt all vintages produced by semiconductor equipment firms. The dotted lines are not the exhaustive list of all vintages. They correspond to only those vintages for which I could obtain data. The data for these were obtained from the websites of semiconductor equipment companies or from industry reports.

5 Explanations for the Acceleration and Slowdown

In this section I use the model to study the acceleration and subsequent slowdown in technological progress, measured as growth of performance. I will argue below that the acceleration was caused by an unanticipated increase in the upstream innovation rate λ, and the slowdown by an unanticipated decrease in the efficiency α with which INTEL used upstream innovations. These explanations are consistent with the model, since it can be seen from equation (16) that an increase in λ increases g_m and a decrease in α decreases g_m. I explore below whether the model's predictions about the response of other variables to unanticipated changes in λ and α are consistent with the data.

The changes in λ do not affect the static policies - $T^*(\ell)$, $m^*(\ell)$, $y^*(\ell)$, c^* or p^*, as can be seen from equations (4)-(10). Such changes do affect the threshold lag x^* in equation (15) and possibly the optimal adoption policy, n^*. To characterize the changes in n^* induced by changes in λ, I use the fact that any change in n^* would affect the present discounted value of the firm. Let $\bar{V}(n,\lambda)$ be the present discounted value of the firm if it adopts every n^{th} innovation, given an arrival rate λ. Clearly, the optimal adoption policy n^* should satisfy

$$n^* = \arg\max_n \ \bar{V}(n,\lambda).$$

As shown in Proposition 3,

$$\bar{V}(n,\lambda) = \frac{1}{\bar{\ell}_0^{\varphi}} \left[\frac{\left\{1 - \left(\frac{\lambda}{\rho+\lambda}\right)^n\right\}\frac{\pi}{\rho} - \left(\frac{1}{\delta^{\varphi}}\frac{\lambda}{\rho+\lambda}\right)^n F(1)}{1 - \left(\frac{1}{\delta^{\varphi}}\frac{\lambda}{\rho+\lambda}\right)^n} \right].$$

I evaluate the expression $\bar{V}(n,\lambda)$ for plausible parameter values of $\{\delta, F(1), \pi, \rho, \varphi, \bar{\ell}_0\}$ for different values of λ and n. Figure 6 shows the result of a sample simulation for $n = \{3,4,5\}$. As can be seen from the figure, n^* is weakly increasing with λ, the intuition for which is provided by the value matching condition in equation (14). An increase in λ increases the value to waiting, the right hand side of equation (14), since the probability of an innovation arriving the next instant in

time is higher. Hence the firm might find it optimal to wait for more innovations to arrive before adopting. The optimal value n^* actually increases only if the increase in λ is sufficiently high. The model thus allows for the possibility that an increase in λ could occur without inducing any change in the adoption policy n^*. If there was an increase in n^* going from Phase I to Phase II then the scaling factor, δ^{n^*}, should have decreased. The scaling factor has not decreased going from Phase I to Phase II, as can be seen from Figure 4. The scaling factor actually increased slightly, suggesting that n^* did not change. The possibility that in going from Phase I to Phase II there was an increase in λ without a change in n^*, finds further support in the data on the time interval between adoptions. Since the adoption interval, $\Delta\tau_j \equiv \tau_j - \tau_{j-1}$, is the time taken for n^* Poisson events to happen, it follows that $\Delta\tau_j \sim \mathbf{G}(n^*, \frac{1}{\lambda})$, where $\mathbf{G}$ is the gamma distribution. The mean adoption interval is then the mean of $\mathbf{G}(n^*, \frac{1}{\lambda})$, which is equal to $\frac{n^*}{\lambda}$. If there was an increase in λ without a change in n^*, then the mean adoption interval, $\frac{n^*}{\lambda}$, should have decreased. The average adoption interval did in fact decrease from 4.35 years in Phase I to 2.10 years in Phase II (this is easily seen in Figure 2).

Next, I examine the model's predictions regarding a change in α. A change in α affects the static optimal policies. A decrease in α does not change the elasticity of $T^*(\ell)$ (which still remains at 2) but decreases the elasticity of $m^*(\ell)$, which is given by $(1 + 2\alpha)$.[21] Indeed, this paper argues that a decrease in the elasticity of $m^*(\ell)$ caused the slowdown in the growth of m, and this decrease is evident in the data (see Table 1). A decrease in α would also reduce the optimal marginal cost c^* and price p^*. Further, it would reduce the elasticity of the revenue function $r^*(\ell)$ and gross profit function $\pi^*(\ell)$, both given by $\varphi = (1 + 2\alpha)(\eta - 1)$ (see equations (11) and (12)). The lack of data on prices, marginal costs and quantity sold makes it difficult to check the predictions of the model against the data for these variables. However revenues and gross profits of INTEL are available from INTEL's annual reports.[22] Table 4 reports the value of φ estimated using the data from annual

[21] Note that in referring to elasticity, I take absolute values, for example the elasticity of $m^*(\ell)$ is $|\frac{\partial m^*(\ell)}{\partial \ell} / \frac{m^*(\ell)}{\ell}|$.

[22] During the years in Phase II and Phase III, most of INTEL's revenues and profits came from sales of microprocessors, and hence the revenues and gross profits reported in annual reports can be taken to be a very close approximation

reports. The elasticity φ decreased from 0.97 in Phase II to 0.26 in Phase III when estimated from the revenue function $r^*(\ell)$, and from 0.99 to 0.28 when estimated from the gross profit function $\pi^*(\ell)$, consistent with the hypothesis that there was a decrease in α in going from Phase II to Phase III. A change in α would also change π (see equation (8)) and hence the threshold lag x^* (see equation 15) and possibly the choice of adoption policy n^* and the scaling factor δ^{n^*}. Similar to the analysis for an unanticipated change in λ above, unless the change in α is sufficiently large, it will not lead to a change in n^*. As can be seen from Figure 4 the scaling factor δ^{n^*} has not changed between Phases II and III, suggesting again that n^* did not change. If neither n^* nor λ changed in going from Phase II to Phase III, then the model predicts that the mean adoption interval $\frac{n^*}{\lambda}$ should not have changed either. This prediction is borne out in the data, the mean adoption interval was 2.03 years in Phase II, quite close to the 2.10 years in Phase III. Thus, the changes seen in the data are consistent with what the model predicts should have been the response of INTEL to an increase in λ in Phase I and a decrease in α in Phase II.

5.1 Decomposition of Changes in Growth of Performance

In this section, I quantitatively assess the contributions of changes in λ and α to the acceleration and slowdown. For two time periods t and t', equation (16) implies that

$$\frac{g_{m_{t'}}}{g_{m_t}} = \left(\frac{\lambda_{t'}}{\lambda_t}\right)\left(\frac{1+2\alpha_{t'}}{1+2\alpha_t}\right). \tag{17}$$

since δ is assumed to be the same across all periods. A change in the rate of technological progress, $\frac{g_{m_{t'}}}{g_{m_t}}$, can thus be neatly separated into contributions from the semiconductor equipment sector, $\frac{\lambda_{t'}}{\lambda_t}$, and from INTEL, $\frac{1+2\alpha_{t'}}{1+2\alpha_t}$. The estimates of α and λ for the three periods, in conjunction with equation (17), can be used to quantitatively decompose the changes in g_m. I estimate the value of λ for the three phases using data on adoption intervals, $\Delta\tau_j$. Since $\Delta\tau_j \sim \mathbf{G}(n^*, \frac{1}{\lambda})$, the parameters n^* and λ can be estimated by the maximum likelihood method using the data on $\Delta\tau_j$. There are,

of the revenues and profits from microprocessor sales.

however, only 13 data points for $\Delta\tau_j$, since INTEL has made just 14 adoptions in the period 1971-2008. Hence the sample for each phase considered separately is very small. Fortunately, the model provides a useful guideline to aid the estimation. The data on the scaling factor implies that n^* has remained constant across the three phases (see stylized fact 1 and Figure 4). Hence I estimate n^* using the data on $\Delta\tau_j$ pooled together from all three phases and use this value of n^* to estimate λ for the three phases separately. For estimating α, equation (6) implies that α can be obtained from the regression, $\ln(m) = constant + (1 + 2\alpha)\ln(\ell)$. The estimates of λ and α are given in Table 1. As can be seen from the table, λ increased after Phase I and α decreased after Phase II.

Table 1: ESTIMATES OF λ and α

	Phase 1	Phase II	Phase III
λ	0.92	1.96	1.90
	(0.27)	(0.47)	(0.47)
α	0.53	0.78	0.14
	(0.18)	(0.10)	(0.02)

Notes: λ is given as the number of innovations per year. λ is estimated using the maximum likelihood method from the data on adoption intervals, which the model predicts to be distributed according to the gamma distribution $G(n^*, \frac{1}{\lambda})$. The parameter α is estimated from the regression $\ln(m) = constant + (1 + 2\alpha)\ln(\ell)$. Standard errors are shown in brackets. Standard errors for λ were estimated by bootstrapping, and are conditional on n^* estimated from the pooled sample.

The decomposition of the acceleration and slowdown into contributions from the two sectors, using the estimated values of λ and α, is shown in Table 2. Note that a contribution of 1 means that

the corresponding sector did not play a role in the acceleration or slowdown. It can be seen from the first row that g_m increased by a factor of 1.79 going from Phase I to II . The contribution from semiconductor equipment industry increased by a factor of 2.13 and the contribution from INTEL increased by factor of 1.24. Hence, the increase in g_m was caused overwhelmingly by an increase in the innovation rate in the semiconductor equipment industry λ.[23] The slowdown, however, was caused entirely by a decrease in INTEL's own efficiency α, as can be seen from the second row of Table 2.

Table 2: Decomposition of the Acceleration and Slowdown

	Change in Rate of Technological Progress	Contribution of Equipment. Co.	Contribution of INTEL
	$\frac{g_{m_{t'}}}{g_{m_t}}$	$\frac{\lambda_{t'}}{\lambda_t}$	$\frac{1+2\alpha_{t'}}{1+2\alpha_t}$
Acceleration	1.79	2.13	1.24
Slowdown	0.46	0.97	0.50

Notes: Equation (16) stipulates that the entries in the second column should equal the product of the entries in the third and fourth columns. A value of 1 for the third or fourth column means that the corresponding sector did not play any role in the change in g_m. As can be seen from the entries in the first row, the equipment firms played the important role in the acceleration. For the slowdown on the other hand, INTEL was responsible and the equipment companies hardly contributed.

[23]The two contributions taken together account for more than the 1.79 factor increase in performance seen in the data, and this discrepancy must be taken to be the result of factors not taken into consideration in this model. One possible explanation for this is that the first adopters of semiconductor equipment during Phase I were DRAM (memory chip) producers and not microprocessor producers. In the later years, microprocessor firms adopted at the same time, if not earlier, than DRAM producers. The presence of possible adoption lags during Phase I would mean that the actual innovation rate λ_1 is lower than the estimated value, which might account for the discrepancy above.

The finding that there was an increase in the innovation rate λ in the semiconductor equipment industry after Phase I has been corroborated in other studies, including Jorgenson (2001) and Aizcorbe et al. (2006), who report it in terms of a decrease in the time interval between the adoption of new vintages. A possible explanation for the increase in λ, suggested in Hutcheson (2005), is that it was the outcome of R&D coordination activities in the semiconductor equipment industry undertaken by SEMATECH, an industrial research consortia established in 1988. It remains a topic of further research to understand the cause of the increase in the innovation rate, and to examine the possible role played by SEMATECH. On the other hand, there is widespread agreement in the semiconductor industry on the reason for the drop in efficiency α, which caused the slowdown. In early 2000s, microprocessors with new designs introduced by INTEL hit a well publicized problem, the microprocessors generated a large amount of heat during their operation which affected their proper functioning. Since then INTEL has abandoned the pattern of design improvements that it had followed in the past and adopted a new approach, the multicore design. The multicore approach is less effective than previous approaches in translating increases in the number of transistors available on a microprocessor to increases in performance. This widely held explanation has found its way even to the popular press, with the following quote coming from an article in the The New York Times - "The computer industry has a secret. Yes, the number of transistors on modern microprocessors continues to multiply geometrically, but no one really knows how to get the most out of all these new transistors". [24] The inability of INTEL's designs to get the most out of the new transistors is captured in the model as a drop in the efficiency α.

Finally, it should be noted that although the explanations for the acceleration and slowdown suggested here are based on shifts in model parameters, there are key relationships in the model that have not changed across the three phases. The scaling factor has remained roughly constant across the three phases (see Figure 4). Similarly, the relationship between T and ℓ has not changed

[24]The quote appeared in an article titled "Optimal Use of Transistors Still Elusive", by John Markoff, in the September 1, 2009 release of The New York Times. The article can be accessed at http://query.nytimes.com/gst/fullpage.html?res=9500E5DC1F38F932A3575AC0A96F9C8B63.

across the three phases (see Figure 5).

6 Conclusion

This paper develops an economic model of the microprocessor industry that endogenizes technological progress in the industry. The model captures well the evolution of different engineering and economic variables in the industry and connects the engineering and economic measures of technological progress. The model was used to understand the cause of the acceleration in technological progress in the industry during 1990-2000 and the subsequent slowdown. Three conclusions emerge from this application of the model. First, the acceleration in technological progress was driven by an increase in the innovation rate in the semiconductor equipment industry leading to more rapid adoption of innovations by INTEL. Second, the slowdown was caused by a decrease in the efficiency with which INTEL was able to use the innovations generated by the semiconductor equipment industry. Third, innovation in the semiconductor equipment industry has been the main workhorse driving technological progress in the microprocessor industry since 2001. However, further innovation in the semiconductor equipment industry is becoming ever more difficult as the industry approaches the physical limit to reducing the size of the transistor. If innovations in the semiconductor equipment industry slows down, then it will accentuate the existing difficulties in maintaining the rate of technological progress in the microprocessor industry.

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7 Mathematical Appendix

Proposition 1 *The optimal policy of the firm is to wait until the lag behind the frontier,* $x = \frac{\bar{\ell}}{\ell}$*, reaches* x^**, where*

$$x^* = \left\{ \left(\rho + \lambda - \frac{\lambda}{\delta^{\varphi}} \right) \left(\frac{v(1) - F(1)}{\pi} \right) \right\}^{\frac{1}{\varphi}}$$

Proof. Equation (13) can be rewritten as

$$v(x) = \frac{\pi}{\rho + \lambda} x^{\varphi} + \frac{1}{\delta^{\varphi}} \frac{\lambda}{\rho + \lambda} \left[Max \left\{ v(\delta x), v(1) - F(1) \right\} \right]$$

where $x \in (0, 1]$. Consider operator, T that maps functions defined on $(0, 1]$ as

$$T(f(x)) = \frac{\pi}{\rho + \lambda} x^{\varphi} + \frac{1}{\delta^{\varphi}} \frac{\lambda}{\rho + \lambda} \left[Max \left\{ f(\delta x), f(1) - F(1) \right\} \right]$$

$T(.)$ maps continuous functions to continuous functions. Moreover, it is easily seen from the conditions in Blackwell (1965) that T is a contraction mapping. Hence by contraction mapping theorem there exists a unique $v(x)$ that solves the Bellman equation above. Moreover, T maps weakly increasing functions to strictly increasing functions, hence $v(x)$ is strictly increasing (see Stokey, Lucas and Prescott (1989)). Hence, there exists a value x^* such that

$$v(x^*) = v(1) - F(1). \tag{18}$$

Moreover, since $v(.)$ is an increasing function and $\delta < 1$

$$v(\delta x^*) < v(1) - F(1). \tag{19}$$

Evaluating the Bellman equation (7) at $x = x^*$ and using equations (18) and 19 gives,

$$\begin{aligned} v(x^*) &= \frac{\pi}{(\rho + \lambda)} x^{*\varphi} + \frac{1}{\delta^{\varphi}} \frac{\lambda}{(\rho + \lambda)} Max \left\{ v(\delta x^*), [v(1) - F(1)] \right\} \\ v(1) - F(1) &= \frac{\pi}{(\rho + \lambda)} x^{*\varphi} + \frac{1}{\delta^{\varphi}} \frac{\lambda}{\rho + \lambda} [v(1) - F(1)] \end{aligned}$$

which gives

$$x^* = \left\{ \left(\rho + \lambda - \frac{\lambda}{\delta^{\varphi}} \right) \left(\frac{v(1) - F(1)}{\pi} \right) \right\}^{\frac{1}{\varphi}}$$

■

Lemma 2 *If* $\Delta\tau_i \sim \mathbf{G}(n^*, \frac{1}{\lambda})$*, then* $E\left[e^{-\rho\Delta\tau_i}\right] = \left(\frac{\lambda}{\rho+\lambda}\right)^{n^*}$

Proof. Since $G(n^*, \frac{1}{\lambda}) = \frac{\lambda^{n^*}\Delta\tau_j{}^{n^*-1}e^{-\lambda\Delta\tau_j}}{\Gamma(n^*)}$, where $\Gamma(n^*) = (n-1)!$ is the Gamma function,

$$\begin{aligned} E\left[e^{-\rho\Delta\tau_i}\right] &= \int_0^\infty e^{-\rho t}\frac{\lambda^{n^*}\Delta\tau^{n^*-1}e^{-\lambda T}}{\Gamma(n^*)}\,d\Delta\tau = \frac{\lambda^{n^*}}{\Gamma(n^*)}\frac{n^*-1}{\rho+\lambda}\int_0^\infty \Delta\tau^{n^*-2}e^{-(\rho+\lambda)\Delta\tau}\,d\Delta\tau \\ &= \left(\frac{\lambda}{\rho+\lambda}\right)^{n^*}\frac{(n^*-1)!}{\Gamma(n^*)} = \left(\frac{\lambda}{\rho+\lambda}\right)^{n^*} \end{aligned}$$

■

Proposition 3 *Given the innovation rate* λ*, the expected present discounted value of adopting every* n^{th} *innovation is*

$$\bar{V}(n,\lambda) = \frac{1}{\bar{\ell}_0^{\varphi}}\left[\frac{\left\{1-\left(\frac{\lambda}{\rho+\lambda}\right)^n\right\}\frac{\pi}{\rho} - \left(\frac{1}{\delta^{\varphi}}\frac{\lambda}{\rho+\lambda}\right)^n F(1)}{1-\left(\frac{1}{\delta^{\varphi}}\frac{\lambda}{\rho+\lambda}\right)^n}\right]$$

Proof. Let $\{\Delta\tau_j\}_{j=0}^{\infty}$ be the adoption intervals. Then the ith adoption with vintage $\ell_i = (\delta^n)^i\,\bar{\ell}_0$, occurs at time $\tau_i = \sum_{j=0}^{i-1}\Delta\tau_j$. Then if the firm follows the policy of adopting every nth innovation, the net profit of the firm in the ith adoption interval (i.e the profit from operating the ith vintage equipment), discounted back to $t=0$ is, $\Pi_i(n,\lambda) =$

$$e^{-\rho\tau_i}\left\{\int_0^{\Delta\tau_i} e^{-\rho t}\frac{\pi}{(\delta^{ni}\bar{\ell}_0)^{\varphi}}\,dt - \frac{F(1)}{(\delta^{ni}\bar{\ell}_0)^{\varphi}}\right\} = e^{-\rho\sum_{k=0}^{i-1}\Delta\tau_k}\frac{1}{\delta^{ni\varphi}\bar{\ell}_0}\left\{\frac{\pi}{\rho}\left(1-e^{-\rho\Delta\tau_i}\right) - F(1)\right\}$$

Then the present discounted value of net profits obtained under the policy of adopting every n^{th} innovation is $\sum_{i=0}^{\infty}\Pi_i(n,\lambda)$, which is given by $\sum_{i=0}^{\infty}\Pi_i(n,\lambda) =$

$$\frac{1}{\bar{\ell}_0^{\varphi}}\left[\sum_{i=0}^{\infty}\frac{1}{\delta^n i\varphi}e^{-\rho\sum_{k=0}^{i-1}\Delta\tau_k}\frac{\pi}{\rho} - \sum_{i=1}^{\infty}\frac{1}{\delta^n i\varphi}e^{-\rho\sum_{k=0}^{i-1}\Delta\tau_k}F(1) - \sum_{i=0}^{\infty}\frac{1}{\delta^n i\varphi}e^{-\rho\sum_{k=0}^{i}\Delta\tau_k}\left(\frac{\pi}{\rho}\right)\right]$$

Then $\bar{V}(n,\lambda) = E\sum_{i=0}^{\infty}\Pi_i(n,\lambda)$

$$= \frac{1}{\bar{\ell}_0^{\varphi}}\left[\sum_{i=0}^{\infty}\frac{1}{\delta^{n^*i\varphi}}\frac{\pi}{\rho}E[e^{-\rho\sum_{k=0}^{i-1}\Delta\tau_k}] - \sum_{i=1}^{\infty}\frac{1}{\delta^{n^*i\varphi}}F(1)E[e^{-\rho\sum_{k=0}^{i-1}\Delta\tau_k}] - \sum_{i=0}^{\infty}\frac{1}{\delta^{n^*i\varphi}}\left(\frac{\pi}{\rho}\right)E[e^{-\rho\sum_{k=0}^{i}\Delta\tau_k}]\right]$$

The adoption interval $\Delta\tau_j$ is the time taken for n^* poisson events to happen. Hence $\Delta\tau_j$ are independent draws from the Gamma distribution $\mathbf{G}(n^*, \frac{1}{\lambda})$. It follows that $\sum_{j=0}^{i-1}\Delta\tau_j \sim \mathbf{G}(n^*i, \frac{1}{\lambda})$. To evaluate the above expectations, I use Lemma 2, which shows that $E\left[e^{-\rho\Delta\tau_i}\right] = \left(\frac{\lambda}{\rho+\lambda}\right)^{n^*}$. This implies

$$\bar{V}(n,\lambda) = E\sum_{i=0}^{\infty}\Pi_i(n,\lambda)$$

$$= \frac{1}{\bar{\ell}_0^{\varphi}}\left[\sum_{i=0}^{\infty}\frac{1}{\delta^{n^*i\varphi}}\frac{\pi}{\rho}\left(\frac{\lambda}{\rho+\lambda}\right)^{n^*i} - \sum_{i=1}^{\infty}\frac{1}{\delta^{n^*i\varphi}}F(1)\left(\frac{\lambda}{\rho+\lambda}\right)^{n^*i} - \sum_{i=0}^{\infty}\frac{1}{\delta^{n^*i\varphi}}\left(\frac{\pi}{\rho}\right)\left(\frac{\lambda}{\rho+\lambda}\right)^{n^*(i+1)}\right]$$

Evaluating the sums of geometric series, the above expression reduces to

$$\bar{V}(n,\lambda) = E\sum_{i=0}^{\infty}\Pi_i(n,\lambda) = \frac{1}{\bar{\ell}_0^{\varphi}}\left[\frac{\left\{1-\left(\frac{\lambda}{\rho+\lambda}\right)^n\right\}\frac{\pi}{\rho} - \left(\frac{1}{\delta^{\varphi}}\frac{\lambda}{\rho+\lambda}\right)^n F(1)}{1-\left(\frac{1}{\delta^{\varphi}}\frac{\lambda}{\rho+\lambda}\right)^n}\right]$$

■

8 Data Sources

The dataset contains the following characteristics for microprocessors made by INTEL - product name, date of release, performance (m), vintage (ℓ), transistors (T). There are a total of 588

microprocessors for INTEL. I omitted the server processors manufactured by INTEL since functionally they are very different from desktop and laptop microprocessors, which form the focus of this paper. The data for m was obtained from two sources - Standard Performance Evaluation Corporation (SPEC) and Business Applications Performance Corporation (BAPCo). SPEC and BAPCO are industry consortia of which both microprocessor producers, INTEL and AMD, are members. The data for T and ℓ were obtained from INTEL website and confirmed against other online reports and articles.

9 Appendix

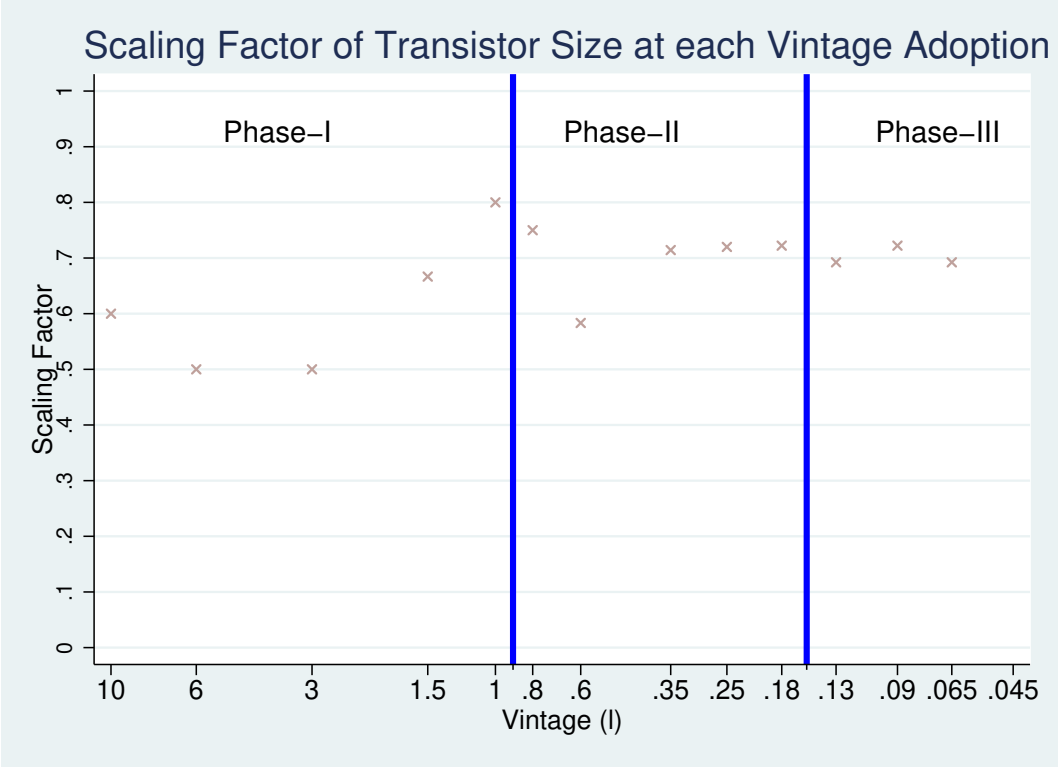

Figure 4: The scaling factor does not show any systematic variation with ℓ.

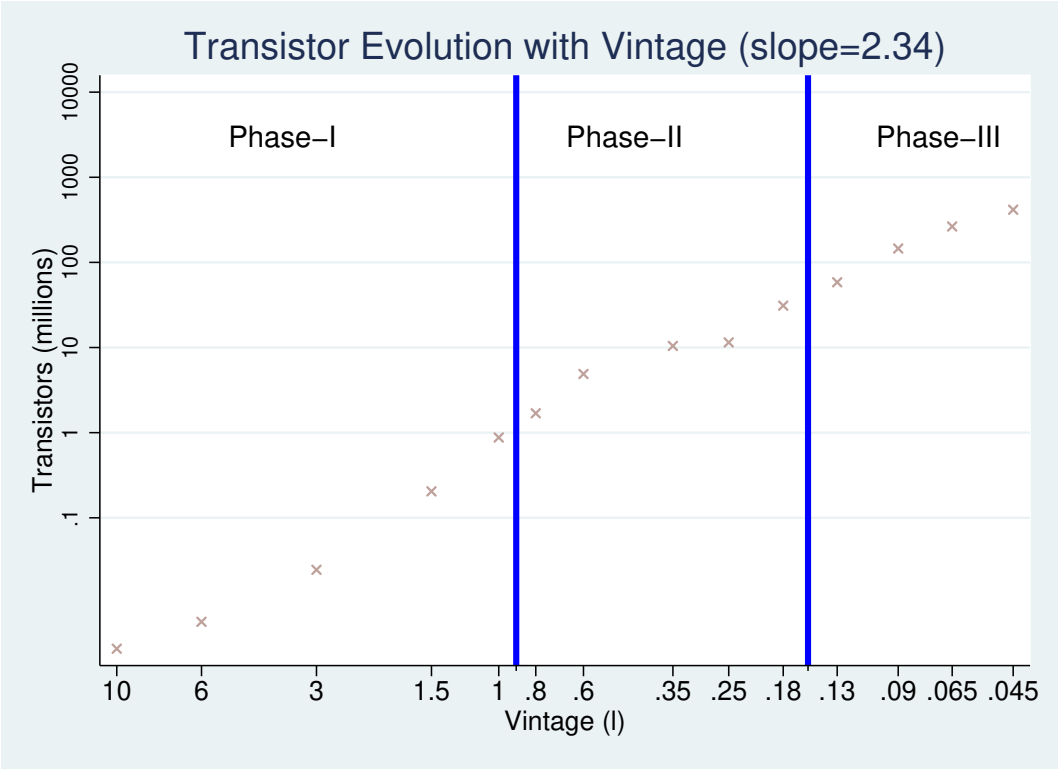

Figure 5: Transistors T increase at roughly double the rate at which ℓ decreases. Note that x-axis values are decreasing to the right.

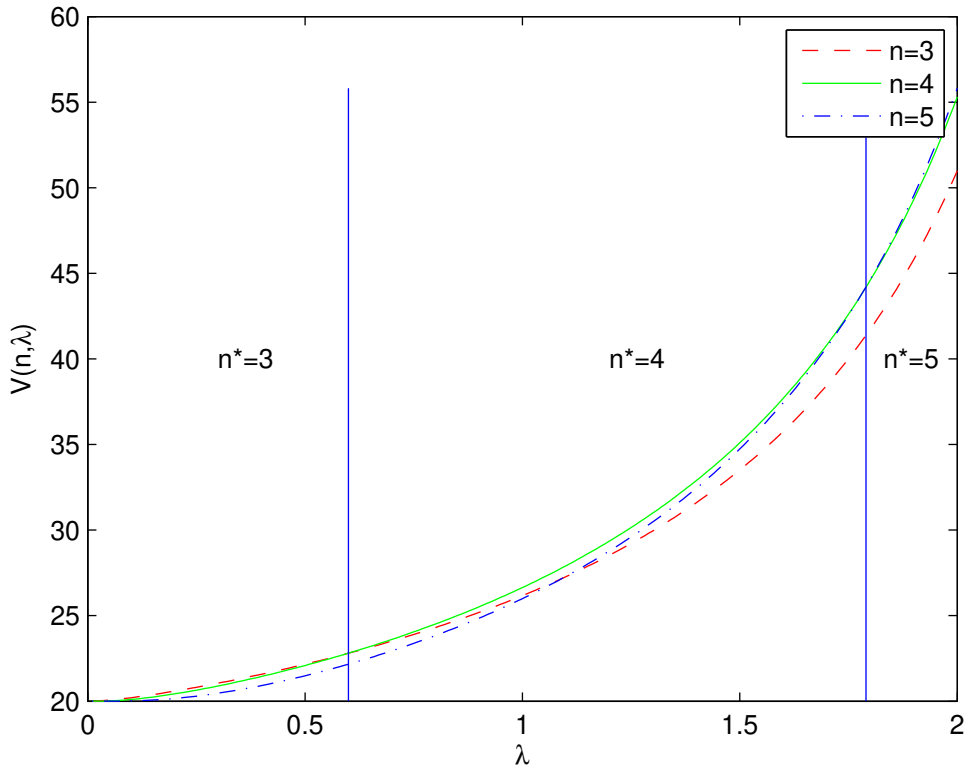

Figure 6: Variation of n^* with λ

Notes: The y-axis variable, $\bar{V}(n, \lambda)$ is the present discounted value of the firm if it adopts every n^{th} innovation, given arrival rate λ. The optimal adoption policy n^* is the value of n that maximizes $\bar{V}(n, \lambda)$. As can be seen from the graph, n^* is weakly increasing in λ.

Table 3: RATE OF TECHNOLOGICAL PROGRESS IN MICROPROCESSOR INDUSTRY

Company	Annual Performance Growth Rate(%)		
	1971-1989	1990-2000	2001-2008
INTEL	28.4	50.2	22.9
AMD	10.9	65.4	18.5

Source: Author

	Annual Hedonic Price Index Decline Rate(%)		
	1988-1994	1994-2001	2001-2004
Industry	30.0	63.1	40.5

Source: Aizcorbe et al. (2006)

Notes: The top panel shows the average growth rate of microprocessor performance during the three phases. The bottom panel shows the rate of decline of price per quality unit given in Aizcorbe et al. (2006) using the hedonic pricing method. As can be seen from the table the growth of performance tracks the decline in price per quality unit.

Table 4: ESTIMATES OF φ FROM THE REVENUE FUNCTION AND GROSS PROFIT FUNCTION

	Phase II	Phase III
Using $r^*(\ell)$	0.97	0.26
	(0.098)	(0.12)
Using $\pi^*(\ell)$	0.99	0.28
	(0.07)	(0.19)

Notes: The first row shows φ estimated from the equation $\ln(r^*) = constant + \ln(\ell)$. The data for revenues were taken from INTEL's annual reports. The average annual revenue over the years of operation of a vintage ℓ is taken as $r^*(\ell)$. The years of operation of a vintage ℓ is taken to be the years between the year in which ℓ was adopted to the year the next vintage was adopted. The second row shows the estimate for φ obtained with a similar approach using the gross profit function $\pi^*(\ell)$.

Table 5: IMPACT ON AGGREGATE PRODUCTIVITY GROWTH

Phase	Output Share of Microprocessors (%)	TFP Growth in Microprocessor Industry (%)	Contribution of Microprocessors to Aggregate TFP Growth (% points)
1971-1989	0.06	28.4	0.017
1990-2000	0.14	50.2	0.070
2001-2008	0.13	22.9	0.031

Notes: The output share is obtained by multiplying the output share of semiconductors given in Oliner and Sichel (2002b) and Oliner, Sichel and J.Stiroh (2007) by a factor of 0.2, which is roughly the share of microprocessors in semiconductor industry revenue. The growth rate of performance is taken as a proxy for the TFP growth in the microprocessor industry. The entry in the fourth column is the product of the entries in the second and third columns. The fourth column represents only the direct contribution of production of microprocessors to aggregate TFP growth, it ignores any indirect effect on aggregate TFP growth through the use of better computers made possible by faster microprocessors.