High Power Two- Stage Class-AB/J Power Amplifier with High Gain and Efficiency

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June 2014

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Abstract

This paper presents a hybrid Broadband power amplifier which provides high drain efficiency. AB and J, Two Classes of power amplifier are described using GaN HEMT with matching networks together with input and output compact elements. Using Load Pull method, the best input and output network in the central frequency of 3.2GHz for output power of 40dBm, 10dB high gain and high efficiency of 80%, has been designed. After describing the design of each of the amplifiers and comparing their performance, the proposed circuit, two-class AB/J are discussed to be the target of the circuit design, reducing the input power to achieve high efficiency output power and gain. Input and output matching proposed circuit elements in terms of theory and simulation are compared, and the results of both investigations were similar. Also, the fundamental harmonic and the second harmonic in the 0.5GHz bandwidth have the desirable amplitude of the output signal.

Index terms

Power Amplifier(PA), High Power, High Drain Efficiency, GaN HEMT, PAE, Broad Band, Class-J, Class-AB, Load Pull, Compact Elements.

Introduction

Universal wireless communication technology has been developed very much in recent decades. The rapid demand of consumers in the broadband bandwidth for smart phones, as well as portable and sufficiently economical mobiles, both in terms of cost and preserving battery

power, has led to the development of these technologies. In 1998, the first CMOS RF power amplifier was made with 1W power delivery at the 2GHz frequency range, with PAE = 41% and 2V power supply [1]. Simultaneously with the developments in the wireless communication industry, tremendous improvements in semiconductor technology emerged. Among them, the most significant progress was the development of CMOS technology. CMOS transistors' remarkable feature is that the speed will increase, while it consumes less power per function than digital and analog circuits which results in reducing the circuit cost and size. Therefore, the ultimate goal of engineers and researchers in the process is putting the power amplifier, IC transmitter and receiver, power management module and digital bandwidth on a piece of Si, GaAs or GaN. Wireless communication systems require high linear power amplifier to send a signal with minimum phase and amplitude distortion. Bandwidth, efficiency, linearity system and desirable output power are four basic and determinant factors for RF microwave power amplifier in the modern communication systems. Improving efficiency and achieving a high output power simultaneously, has proposed a useful design method which is a promising solution, using various classes of power amplifier (Single or Mix). Usually, power amplifiers are based on their configuration and their performance conditions, and are classified in various classes (eg, Class A, B, C, AB, D, F, F^{-1}, S, G, J, etc). Classes A, B, C, AB, depending on the conduction angle, are chosen and dealt with increasing linearization circuit by reducing efficiency and increasing conduction angle [1-3]. In [4] a comparison between the two classes AB and J is done at a frequency of 0.7GHz which is designed on the SiGe transistors device. Our proposed method is the design of a two-stage power amplifier with merging two classes AB and J to improve four main factors of the power amplifier.

At first, the GaN transistor is analyzed; the next two sections will describe the classes AB and J. Finally the performance of the proposed class AB/J power amplifier will be explained and is compared to each of the classes AB and J. Then the final results will be discussed in the conclusion.

Analysis of transistor GaN CGH40010F

According to the designer's tendency to use a broadband power amplifier, together with taking into account to pay more in the making GaN transistor, it was to use GaN transistor for designing a two stage proposed power amplifier. Designers believe that GaN transistors are used

in HEMT's Hetero structure. By comparison, the different substrates of the power amplifier design are done. The result was that perfect choice for the first and second stage transistors of proposed circuit is GaN transistor [2, 4, 5].

Table I.
The comparison between different substrates for power amplifier transistor design

Band Gap Energy	(eV)	Si(1.13)⟨GaAs(1.4)⟨GaN(3.4)
Breakdown E Field	(MV/cm)	GaAs(0.4)⟨Si(0.5)⟨GaN(3.0)
Saturated Velocity	(cm/s)	$Si(1.08\times10^7)\langle GaAs(1.3\times10^7)\langle GaN(2.7\times10^7)$

To use GaN transistors, due to new technology, in the ADS software, these transistors must be defined so that the bias point defined is compared with bias point in Datasheet. According to studies, classes AB and J with Broad Band bandwidth within the GHz range have high efficiency and output power. For selection bias point of the transistor using GaN circuit schematic and simulation in ADS, using the tools "FET Curve Tracer", at the I_{DS} = 0.5A and V_{DS} = 28V, the circuit is designed at the central frequency of 3.2GHz. Also DC power for input stage "Class-AB" and output stage, "Class- J" is equal to 14V. For the analysis S parameters of Table II at the for GaN CGH40010F transistor are used.

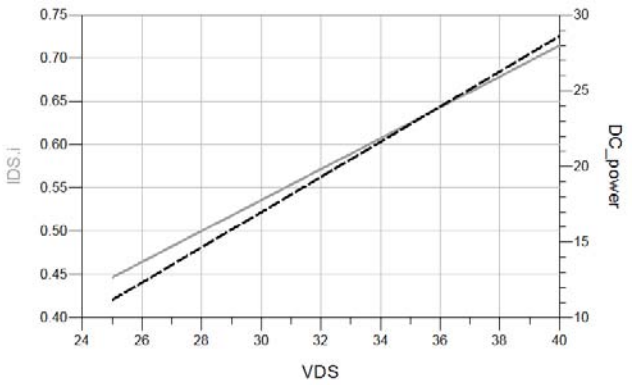

Fig. 1. Determining the bias point and DC power transistor.

Table II.
S parameters analysis at the 1GHz-5GHz frequency range for GaN transistor

freq	S(1,1)	S(1,2)	S(2,1)	S(2,2)
1.000 GHz	0.902 / -163.934	0.021 / 1.908	9.922 / 82.409	0.313 / -147.540
2.000 GHz	0.900 / 172.303	0.020 / -13.758	5.036 / 56.056	0.366 / -159.351
3.000 GHz	0.900 / 155.938	0.018 / -22.462	3.384 / 33.968	0.424 / -169.017
4.000 GHz	0.900 / 139.964	0.017 / -25.619	2.583 / 12.737	0.471 / 179.261
5.000 GHz	0.898 / 122.271	0.016 / -23.489	2.132 / -8.895	0.503 / 165.109

Design class-AB

The purpose of selecting a class AB as the first stage was its very low distortion against classes B and C. The two-stage power amplifier, often tend to use four classes A, B, AB, C for first-stage design. Class AB has several KW output power and can provide the required input power for the second stage. Another two-stage power amplifier design goals is to reduce the input power or P_{in}, because the power amplifier should be directed to more output power with the lower input power. For input and output matching and design Class AB are used from Load And Source Pull and high-Pass L-Type techniques. 50 Ω Output resistance and 3.2GHz central frequency and GaN CGH40010F transistors, are selected. voltage supply of the drain and gate and Choke inductors are used for biasing the proposed circuit. (V_{gs}=-2.25V,V_{ds}=28V) The difference proposed circuit with other power amplifier in its gate bias. To increase the gate, voltage bias circuit of Fig. 2 has been used. Because of the used bias circuit, the transistor gate voltage is increased; that's because the bias circuit at P_{in} = 33dBm, leading to high efficiency above 80%, at the gate, voltage is equal to 4.6V, but without the proposed bias circuit, the voltage is reduced to 3.3V.

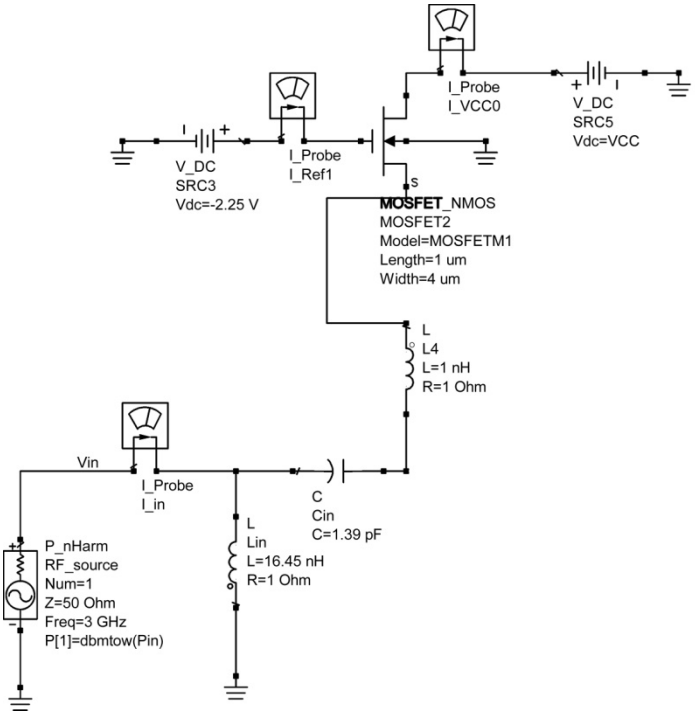

Fig. 2. The proposed bias circuit to increase the gate supply voltage on the first stage of the power amplifier

The Load and Source Pull method, using the harmonic balance analysis, will achieve the best PAE and power delivered to load, and then according to this, the matching circuit is implemented with compact elements based on class AB power amplifier configuration. Load and Source Pull analysis provides optimum input impedance 202.620-j152.585 and output impedance 51.849-j10.483 for Class AB power amplifier circuit's transistor. By implementing this method in input and output, PAE of 40% and power delivered to load is about 40dBm. Note that the high output power is achieved at the cost of losing efficiency.

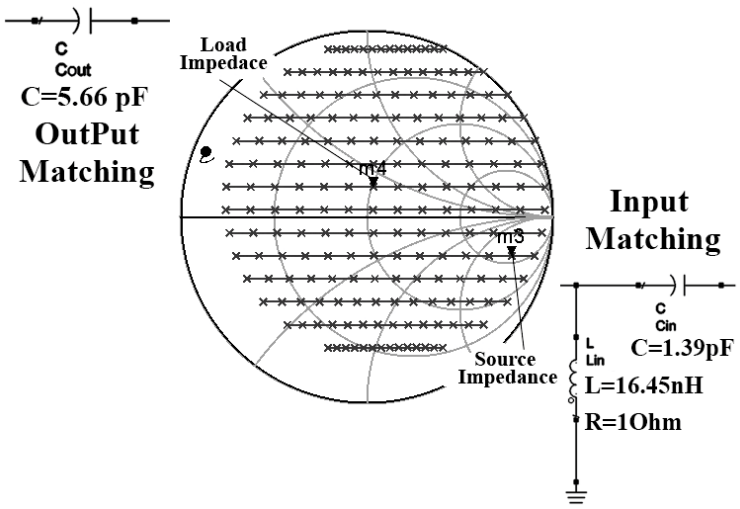

Fig. 3. input and output matching using Load and Source Pull method in class-AB.

In order to account stability coefficients of the circuit, the following table is needed; it must be stabfact⟩1 , stabmeas⟩0 that occurs in up to 3.100GHz frequency. Then center frequency is chosen correctly.

Table III.
S Parameters analysis in the 3GHz-3.5GHz frequency range for GaN transistor

freq	StabFact1	StabMeas1
3.000 GHz	0.971	1.569
3.100 GHz	1.010	1.551
3.200 GHz	1.051	1.537
3.300 GHz	1.092	1.526
3.400 GHz	1.133	1.519
3.500 GHz	1.176	1.514

If I_g and V_g curve is to obtain the input impedance of the transistor, the real input impedance will not be negative, so to compensate for the real impedance of the transistor, it will not put the resistance at the input after the compact elements.

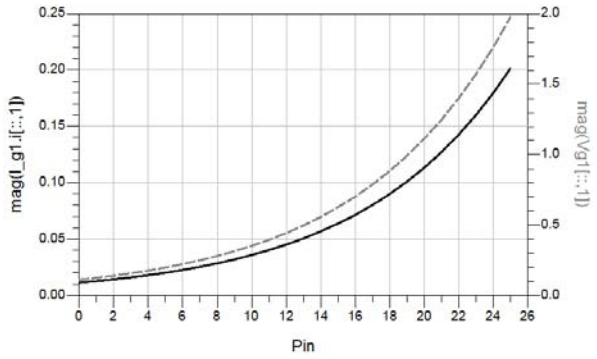

Fig. 4. Diagram of gate current and voltage against input power to obtain the real input impedance of the transistor.

Choke inductor and output capacitor are used as a path for the dc power supply. Using the equations in [6], output matching parameters are also calculated in the following way. According to 8W output power at P_{in} = 29dBm, using equation (1), R_{out} should be designed in order to close the $50\ \Omega$ output resistance. We calculated in the power supply of 28V which is equal to $50\ \Omega$.

$$R_{out} = \frac{\left(V_{CC} - V_{sat}\right)}{2 \times P_{out}} \qquad (1)^{[6]}$$

To determine the output parameters, Q_L = 1.8 is calculated, and considering the $5\ \Omega$ load resistor, the output capacitor is 5.8 pF based on equation (2) which is a little more that the amount specified in the Load Pull technique. Getting the output inductor from equation (3), for compensating the output capacitor at the central frequency, we should parallel a large and arbitrary inductor with that output inductor; as a result the Choke inductor is 1nH.

$$C = \frac{1}{R \times Q_L \times \omega} \qquad (2)^{[6]}$$

$$L = \frac{R_{out}}{Q_L \times \omega} \qquad (3)^{[6]}$$

Design class-J

Class-J has been proposed recently by a linear function, if it terminates to the appropriate fundamental and second harmonics, we will certainly have higher efficiency from class AB. For this reason, the Class- J is called "class deep AB" or "Class AB at high frequency" [7]. Hence, there must be a great accuracy on the selection of input termination until output component of the second harmonic with the proper phase will be achieved. In order to achieve high efficiency and power output in Class-J, this class has been introduced as an Output stage of the proposed power Amplifier. In this class Load and Source Pull techniques are used for matching impedance at the fundamental and second harmonics. Also for the bias circuit V_{gs} =-2.25V and V_{ds} = 28V are used, which is series with a 20nH Choke inductor with 1 Ω dissipation. Point to note is that after checking the result on the stability of the circuit using Table IV, which is about the Class-J power amplifier design with compact elements, in terms of stability it is much better than class-AB power amplifier.

Table IV.
S Parameters analysis in the 3GHz-3.5GHz frequency range for GaN transistor

freq	StabFact1	StabMeas1
3.000 GHz	3.204	1.355
3.100 GHz	3.058	1.341
3.200 GHz	2.900	1.322
3.300 GHz	2.734	1.300
3.400 GHz	2.564	1.274
3.500 GHz	2.394	1.244

Load and Source Pull analysis for the class-J power amplifier are designed to get optimum input impedance 9.605-j1.336 and output impedances 14.088-j7.016 for transistor. Also, about 50% PAE and 40dBm of power delivered to load is selected for the design of compact elements in the Smith Chart.

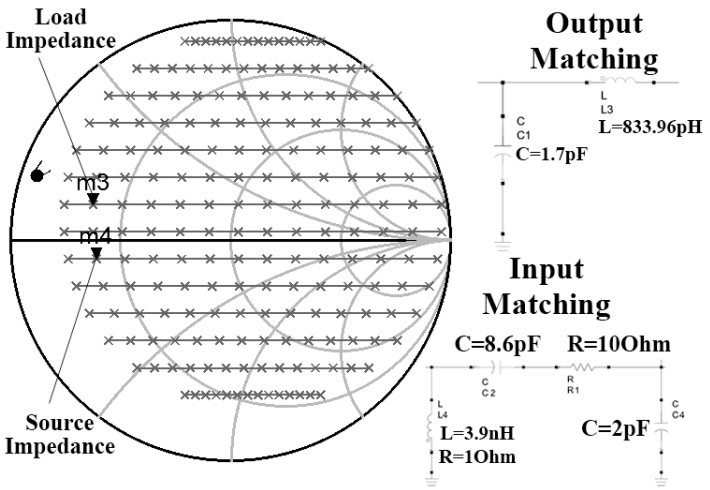

Fig. 5. Input and output matching in class-J using Load and Source Pull method.

In explaining the output circuit design for power amplifier this fact should be pointed out that output capacitance should be chosen carefully so that in the higher harmonic frequencies it is approximated as a short circuit. After the design of the output matching network, the ratio of capacitive reactance to the resistance of the load line should be calculate [8]. If this ratio is equal to or less than unity, our design will be ideal. Also depending on the frequency and device technology, this ratio can be achieved above the unit [8]. In this paper in considering the $R_L = 25\ \Omega$ and GaN transistor, this ratio is $\frac{X_{C_{ds}}}{R_L} = 1.2$.

In the theoretical analysis of the fundamental and second harmonic impedances for class-J power amplifier is used from the following equation.

$$\begin{cases} Z_{F_1} = R_{Opt} + jR_{Opt} & (4)^{[8]} \\ Z_{F_2} = -j\frac{3\pi}{8}R_{Opt} & (5)^{[8]} \\ R_{Opt} = \frac{2\times(V_{DC} - V_K)}{I_{max}} & (6)^{[8]} \end{cases}$$

Based on the Load Pull results, fundamental and second harmonic impedances compared with its theoretical values and are listed in Table V.

Table V.

Achieving the maximum output power at fundamental and second harmonic at the 3.2GHz center frequency

	P_{out}(dBm)	Load pull	Theory
Fundamental Impedance	41.752	14.088+j7.016	21+j21
Second Harmonic Impedance	42.252	-j25.067	-j24.7275

Simulation results

After the first and second stage of designing the power amplifier, and combining two stages as a proposed circuit, the simulation results are listed in Table VI. As you can see, the purpose of the proposed power amplifier design is to reduce the input power to obtain maximum efficiency and power output. The unique characteristic of the two-stage circuit is the input power has decreased about 10dBm compared to other stages. It should be noted that when calculating the PAE, the whole current of the dc circuit and calculating Drain Efficiency, just output DC current are intended. A comparisons of the previous works with the proposed method are shown in the following tables.

Table VI.

Comparison of the simulation results of the first and second stage of the amplifier with final two stage power amplifier

	P_{in}(dBm)	P_{out}(dBm)	Gain(dB)	PAE(%)	Drain Efficiency(%)
First Stage	33	43.213	10.213	72.259	86.172
Second Stage	29.5	41.252	11.752	74.688	82.690
Final circuit	17.5	41.307	23.807	54.181	83.842

Table VII.

Comparison of the simulation results of the first and second stage of the amplifier with previous work done

Class	J	J	J	J	J	AB	J	AB/J
Year[Ref]	2013[3]	2013[7]	2013[9]	2012[10]	2011[11]	This Work	This Work	This Work
Bandwidth (GHz)	1.6-3	2.2-3.07	0.8-1.9	2.6-3.3	0.6-2.4	2.9-3.4	2.9-3.4	2.9-3.4
Technology	**CGH40010F**	**GaN 0.5W**	**CGH40045F**	**GaN HEMT**	**CGH40010F**	**CGH40010F**	**CGH40010F**	**CGH40010F**
Voltage supply (V)	28	15	28	25	28	28	28	28
Efficiency (%)	60-75	72	68	55	63	86.172	82.690	83.842

Table VIII.

Comparison between the switching classes and class J at the different parameters

Device	**F_0 (GHz)**	**Pout (W)**	**V_{DC} (V)**	**PAE (%)**	
GaN HEMT	2.00	11.5	50	74.3	Class-E[12]
GaN HEMT	2.10	11.2	50	79.7	Class-E[12]
GaN HEMT	2.14	12	40	74	Class-E[12]
GaN HEMT	2	16.5	42.5	85.5	Class-F[12]
GaN HEMT	2.10	12	28	79.6	Class-F^{-1}[12]
GaN HEMT	2.14	11.5	30	77.3	Class-J[12]
GaN HEMT	3	13.34	28	74.688	Class-J[This Work]

According to the first and third harmonics of the circuit in Fig. 6, the minimum output power parameter of the fundamental harmonic is 38.256dBm and the maximum is 39.497dBm, Which at the range of 2.9-3.4GHz bandwidth it is equal to or greater than 38dBm which is desirable for the design.

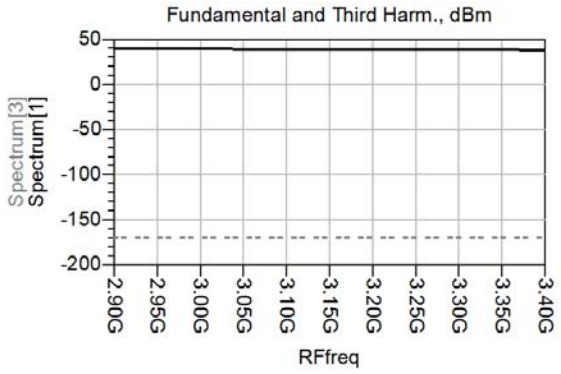

Fig. 6. Output power parameters analysis of the first and third harmonics.

As shown in Fig. 7, PAE characteristic of the proposed power amplifier during the whole frequency bandwidth changes the minimum 58.570% to the maximum 77.785%. Power gain transducer characteristic is variable at the 24.256dB-25.497dB , due to the level of the input power is greater than 15dBm, and the level of output power will be greater than 38dBm. Also according to this analysis the output power is about 12.5W at the fundamental harmonic and dc power dissipation which is defined with power dissipation of the power supply that biases the gate and drains the transistor, about 10W is achieved. Also 20% of these dissipations are because of the changes in PAE.

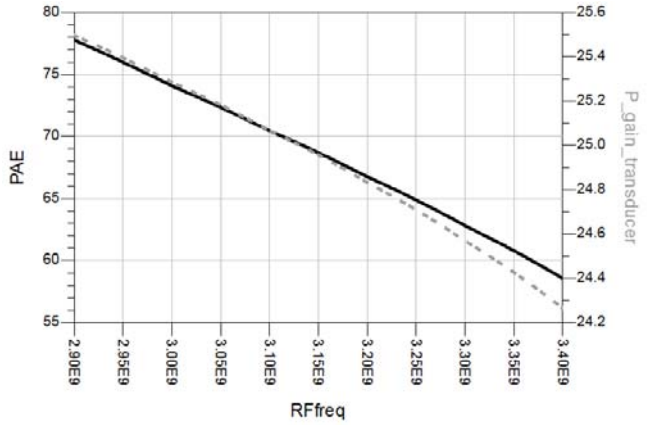

Fig. 7. Analysis of PAE and % power gain transducer at the 0.5GHz frequency range.

Output spectrum that includes signals at the fundamental and second harmonic frequencies is shown in Fig. 8(a). Fundamental signal amplitude at the 3.2GHz frequency is 37.807dBm and second harmonic amplitude at the 6GHz frequency is equal to -377.180dBm. The smaller is the negative number of the output harmonic amplitudes, the closer will be output signal to a sine wave that is shown in Fig. 8(b). Also to get the harmonics dBc value of the fundamental frequency signal, the signal amplitude of the fundamental frequency are subtracted from the second harmonic amplitude so the result will be equal to -414.987dBc.

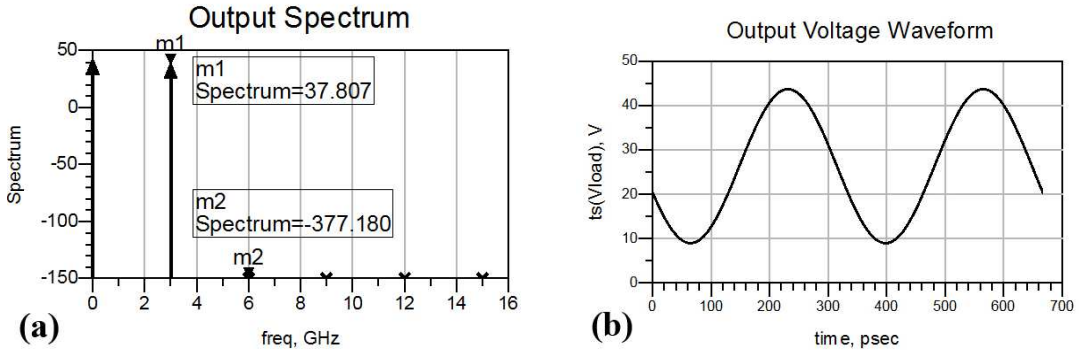

Fig. 7. (a) Output spectrum at the fundamental and second harmonic frequency. (b) The output voltage waveform is close to sine.

Conclusion

A new and proposed two-stage class AB/J circuit analysis is performed in this paper. Conspicuous feature is 10dBm size reduction of the input power compared with each class, in order to obtain the maximum power delivered to load and the efficiency above 80% of the circuit. Precise analysis explains mechanism of classes AB and J operation which are some types of power amplifiers. Based on Load and Source Pull method, harmonic matching has been done for input and output network by compact elements to increase drain efficiency. In this proposed amplifier at 2.9GHz-3.4GHz frequency range, PAE has increased more than 60% and the circuit has a gain of 24dB. Therefore, two-stage power amplifier with GaN transistors can be useful for applications with less input power at Broad band bandwidth.

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